

## CLAIMS

1           1.     A digital data processing apparatus, comprising:  
2                 at least one processor, each said at least one processor executing at least one  
3                 respective thread of processor-executable instructions, said at least one processor collectively  
4                 including:

5                     (a) a plurality of parallel pipelines, each pipeline of said plurality of parallel  
6                     pipelines having the capability to perform a set of pre-defined functions on respective  
7                     input data; and

8                     (b) control logic controlling the routing of data to said plurality of parallel  
9                     pipelines, wherein said control logic, responsive to detection of a failure of a first  
10                    pipeline of said plurality of parallel pipelines, causes data intended for processing by  
11                    said first pipeline to be processed by a second pipeline of said plurality of parallel  
12                    pipelines.

1           2.     The digital data processing apparatus of claim 1, wherein said plurality of parallel  
2                 pipelines comprises at least one redundant pipeline.

1           3.     The digital data processing apparatus of claim 2, wherein said plurality of parallel  
2                 pipelines comprises N primary pipelines and a single redundant pipeline, said redundant  
3                 pipeline providing redundant function in the event of failure of any single one of said N  
4                 primary pipelines, where N is greater than 1.

1           4.     The digital data processing apparatus of claim 1, wherein said control logic comprises  
2                 selection logic at one or more inputs to each respective pipeline, said selection logic  
3                 controlling the selection between a primary source and a secondary source of pipeline data  
4                 for the respective pipeline.

1 5. The digital data processing apparatus of claim 4, wherein said selection logic is  
2 integrated with operand source selection logic for one or more stages of the respective  
3 pipeline.

1 6. The digital data processing apparatus of claim 1, wherein said at least one processor  
2 is a plurality of processors, said plurality of processors sharing at least one of said plurality  
3 of parallel pipelines.

1 7. The digital data processing apparatus of claim 6, wherein said plurality of processors  
2 shares a redundant pipeline of said plurality of parallel pipelines.

1 8. The digital data processing apparatus of claim 1, wherein  
2 said plurality of pipelines is arranged in an array;  
3 said control logic, responsive to detection of a failure in said first pipeline, causes  
4 data intended for processing by said first pipeline to be processed by said second pipeline,  
5 said second pipeline being physically adjacent said first pipeline in said array; and  
6 said control logic, responsive to detection of a failure in said first pipeline, further  
7 causes data intended for processing by said second pipeline to be processed by a third  
8 pipeline of said plurality of parallel pipelines, said third pipeline being physically adjacent  
9 said second pipeline in said array.

1 9. The digital data processing apparatus of claim 1, wherein said plurality of parallel  
2 pipelines perform arithmetic operations on floating point data.

1 10. The digital data processing apparatus of claim 9, wherein said plurality of parallel  
2 pipelines perform arithmetic operations on mixed data, including floating point data and  
3 fixed point data.

1 11. The digital data processing apparatus of claim 1, further comprising:  
2 a plurality of processors;  
3 a memory storing instructions for execution on said plurality of processors; and  
4 at least one bus coupling said plurality of processors to said memory.

1 12. A processor, comprising:  
2 a plurality of parallel pipelines, each pipeline of said plurality of parallel pipelines  
3 having the capability to perform a set of pre-defined functions on respective input data, said  
4 plurality of parallel pipelines including at least one redundant pipeline; and  
5 control logic controlling the routing of data to said plurality of parallel pipelines,  
6 wherein said control logic, responsive to detection of a failure of a first pipeline of said  
7 plurality of parallel pipelines, causes data intended for processing by said first pipeline to be  
8 processed by a second pipeline of said plurality of parallel pipelines.

1 13. The processor of claim 12, wherein said plurality of parallel pipelines comprises N  
2 primary pipelines and a single redundant pipeline, said redundant pipeline providing  
3 redundant function in the event of failure of any single one of said N primary pipelines,  
4 where N is greater than 1.

1 14. The processor of claim 12, wherein said control logic comprises selection logic at one  
2 or more inputs to each respective pipeline, said selection logic controlling the selection  
3 between a primary source and a secondary source of pipeline data for the respective pipeline.

1 15. The processor of claim 14, wherein said selection logic is integrated with operand  
2 source selection logic for one or more stages of the respective pipeline.

1 16. The processor of claim 12, wherein  
2 said plurality of pipelines is arranged in an array;

1           said control logic, responsive to detection of a failure in said first pipeline, causes  
2 data intended for processing by said first pipeline to be processed by said second pipeline,  
3 said second pipeline being physically adjacent said first pipeline in said array; and

4           said control logic, responsive to detection of a failure in said first pipeline, further  
5 causes data intended for processing by said second pipeline to be processed by a third  
6 pipeline of said plurality of parallel pipelines, said third pipeline being physically adjacent  
7 said second pipeline in said array.

1           17.   The processor of claim 12, wherein said plurality of parallel pipelines perform  
2 arithmetic operations on floating point data.

1           18.   The processor of claim 17, wherein said plurality of parallel pipelines perform  
2 arithmetic operations on mixed data, including floating point data and fixed point data.